IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **ROCHE ET AL.** Serial No. **Not Yet Assigned** Filing Date: **Herewith** For: **MICROPROCESSOR COMPRISING AN INSTRUCTION FOR INVERTING BITS IN A BINARY WORD**	I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231. EXPRESS MAIL NO: EL747059878US DATE OF DEPOSIT: February 6, 2002 NAME: Dawn Kimler SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 6.

Please add new Claims 7 to 35.

7. A microprocessor comprising:
a central processing unit comprising
a plurality of registers,
an arithmetic and logic unit having a plurality

of inputs and one output being fed back to one of said plurality of inputs through a data path, said arithmetic and logic unit performing arithmetic and logic operations on binary words stored within said plurality of registers,

a shift unit in the data path for performing shift operations on bits of a binary word being supplied thereto, and for selecting a shift operation to be performed, and

an inverting unit in the data path for inverting an order of the bits of the binary word.

8. A microprocessor according to Claim 7, wherein said shift unit is upstream from said arithmetic and logic unit.

9. A microprocessor according to Claim 7, wherein said shift unit is downstream from said arithmetic and logic unit.

10. A microprocessor according to Claim 7, wherein said shift unit comprises:

a bus comprising a plurality of lines equal in number to a number of the bits in the binary word to be processed; and

a plurality of demultiplexers equal in number to the number of bits in the binary word to be processed, each demultiplexer having an input for receiving one respective bit of the binary word being input to said shift unit, and having a plurality of outputs connected to a respective line of said bus and being equal in number to a number of shift operations

to be performed, with one of said plurality of outputs being selected as a function of the shift operation for providing a value of the respective input bit.

11. A microprocessor according to Claim 10, wherein a line of said bus to which each output of each demultiplexer is connected is chosen in accordance with a rank, within the binary word to be processed, of the respective bit input to said demultiplexer and with the shift operation corresponding to the output of the demultiplexer.

12. A microprocessor according to any of Claim 7, wherein said inverting unit is upstream from said shift unit.

13. A microprocessor comprising:

a plurality of registers;

an arithmetic and logic unit having a plurality of inputs and one output being fed back to one of said plurality of inputs through a data path, said arithmetic and logic unit performing arithmetic and logic operations on binary words stored within said plurality of registers;

a shift unit in the data path for performing shift operations on bits of a binary word being supplied thereto, and

an inverting unit in the data path for inverting an order of the bits of the binary word.

14. A microprocessor according to Claim 13, wherein said shift unit selects the shift operations to be performed.

15. A microprocessor according to Claim 13, wherein

said inverting unit selects the inversion operation to be performed.

16. A microprocessor according to Claim 13, wherein said shift unit is upstream from said arithmetic and logic unit.

17. A microprocessor according to Claim 13, wherein said shift unit is downstream from said arithmetic and logic unit.

18. A microprocessor according to Claim 13, wherein said shift unit comprises:

a bus comprising a plurality of lines equal in number to a number of the bits in the binary word to be processed; and

a plurality of demultiplexers equal in number to the number of bits in the binary word to be processed, each demultiplexer having an input for receiving one respective bit of the binary word being input to said shift unit, and having a plurality of outputs connected to a respective line of said bus and being equal in number to a number of the shift operations to be performed, with one of said plurality of outputs being selected as a function of a shift operation to be performed for providing a value of the respective input bit.

19. A microprocessor according to Claim 18, wherein a line of said bus to which each output of each demultiplexer is connected is chosen in accordance with a rank, within the binary word to be processed, of the respective bit input to

said demultiplexer and with the shift operation corresponding to the output of the demultiplexer.

20. A microprocessor according to any of Claim 13, wherein said inverting unit is upstream from said shift unit.

21. A microprocessor comprising:

a plurality of registers;

a logic unit having a plurality of inputs and one output being fed back to one of said plurality of inputs through a data path, said logic unit performing logic operations on binary words stored within said plurality of registers;

a shift unit in the data path for performing shift operations on bits of a binary word being supplied thereto, said shift unit comprises

a bus comprising a plurality of lines equal in number to a number of the bits in the binary word to be processed,

a plurality of demultiplexers equal in number to the number of bits in the binary word to be processed, each demultiplexer having an input for receiving one respective bit of the binary word being input to said shift unit, and having a plurality of outputs connected to a respective line of said bus and being equal in number to a number of shift operations to be performed; and

an inverting unit in the data path for inverting an order of the bits of the binary word.

22. A microprocessor according to Claim 21, wherein

one of said plurality of outputs of each demultiplexer is selected as a function of a shift operation to be performed for providing a value of the respective input bit.

23. A microprocessor according to Claim 21, wherein said shift unit selects the shift operations to be performed.

24. A microprocessor according to Claim 21, wherein said inverting unit selects an inversion operation to be performed.

25. A microprocessor according to Claim 21, wherein said shift unit is upstream from said logic unit.

26. A microprocessor according to Claim 21, wherein said shift unit is downstream from said logic unit.

27. A microprocessor according to Claim 21, wherein a line of said bus to which each output of each demultiplexer is connected is chosen in accordance with a rank, within the binary word to be processed, of the respective bit input to said demultiplexer and with a shift operation to be performed corresponding to the output of said demultiplexer.

28. A microprocessor according to any of Claim 21, wherein said inverting unit is upstream from said shift unit.

29. A method for manipulating bits in a binary word within a microprocessor comprising a plurality of registers, and a logic unit having a plurality of inputs and one output being fed back to one of the plurality of inputs through a

data path, the method comprising:

performing shift operations in the data path on bits of a binary word being supplied to the logic unit based upon a selected shift operation; and

inverting an order of the bits of the binary word in the data path.

30. A method according to Claim 29, further comprising selecting the shift operation.

31. A method according to Claim 29, wherein the shift operations are performed upstream from the logic unit.

32. A method according to Claim 29, wherein the shift operations are performed downstream from the logic unit.

33. A method according to Claim 29, wherein the shift operations are performed using a shift unit comprising a bus having a plurality of lines equal in number to a number of the bits in the binary word to be processed, and a plurality of demultiplexers equal in number to the number of bits in the binary word to be processed, each demultiplexer having an input and a plurality of outputs connected to a respective line of the bus and being equal in number to a number of shift operations to be performed, the method further comprising:

providing one respective bit of the binary word being input to the shift unit to an input of each demultiplexer; and

selecting one of the plurality of outputs of each demultiplexer as a function of a shift operation to be performed for providing a value of the respective input bit.

34. A method according to Claim 33, wherein a line of the bus to which each output of each demultiplexer is connected is chosen in accordance with a rank, within the binary word to be processed, of the respective bit input to the demultiplexer and with the shift operation to be performed corresponding to the output of the demultiplexer.

35. A microprocessor according to any of Claim 29, wherein the shift operations are performed using a shift unit, and wherein the inverting is performed in an inverting unit upstream from the shift unit.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

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ROCHE ET AL.
Serial No. **Not Yet Assigned**
Filed: **Herewith**

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Respectfully submitted,

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